MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

Labor Mikroelektronik-Vertiefung (EIT-EMS-656-L-4) Embedded Processor Lab (EIT-EMS-546-L-4)

Summer Semester 2017

Organization

Uwe Wasenmüller

TECHNISCHE UNIVERSITÄT KAISERSLAUTERN

MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

Overview

- Tasks of the labs
- Acceptance tests
- Schedule & dates
- Group building rules
- Access to computers
- Contacts; Questions & Answers
- Group building

Tasks

1. Mikroelektronik-Vertiefer Labor:
   - V1-V3 -> download from AG König website
   - Additional task of AG König will be given later
   - Contact: Chetan Dobariya chetandobariya1993 @ gmail.com
   - V4-V5, V7-V8 -> download from lab website
   - Further documentation (print-out) for V4-V8 available now

2. Embedded Processor Lab:
   - V4-V5 -> download from lab website
   - V6_E-V7_E -> download from lab website

3. Embedded Processor Lab & Mikroelektronik-Vertiefer Labor:
   - not applicable

Acceptance Tests

- On Tuesdays, **Wednesdays** & Thursdays 14:00 – 18:00
- Max. one retry per task
- Max. two retries for complete lab
- For preferred time of acceptance test for each task a separate sheet will be available in 12/274 every week
- Schedule for acceptance tests see separate Excel Sheet

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Schedule for Acceptance Tests MEL

Lecture week	Tuesday	Wednesday	Thursday	Remarks	Task
1	18.04.2017	19.04.2017	20.04.2017		
2	**25.04.2017**	26.04.2017	27.04.2017	KICK OFF	
3	02.05.2017	03.05.2017	04.05.2017		
4	09.05.2017	10.05.2017	11.05.2017		
5	16.05.2017	17.05.2017	18.05.2017		V4
6	23.05.2017	24.05.2017	25.05.2017		
7	30.05.2017	31.05.2017	01.06.2017		V5
8	06.06.2017	07.06.2017	08.06.2017		V7
9	13.06.2017	14.06.2017	15.06.2017		V8
10	20.06.2017	21.06.2017	22.06.2017		
11	27.06.2017	28.06.2017	29.06.2017		V1
12	04.07.2017	05.07.2017	06.07.2017		V2
13	11.07.2017	12.07.2017	13.07.2017		V3
14	18.07.2017	19.07.2017	20.07.2017		New task

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Schedule for Acceptance Tests EPL

Lecture week	Tuesday	Wednesday	Thursday	Remarks	Task
1	18.04.2017	19.04.2017	20.04.2017		
2	**25.04.2017**	26.04.2017	27.04.2017	KICK OFF	
3	02.05.2017	03.05.2017	04.05.2017		
4	09.05.2017	10.05.2017	11.05.2017		
5	16.05.2017	17.05.2017	18.05.2017		V4
6	23.05.2017	24.05.2017	25.05.2017		
7	30.05.2017	31.05.2017	01.06.2017		V5
8	06.06.2017	07.06.2017	08.06.2017		
9	13.06.2017	14.06.2017	15.06.2017		V6E
10	20.06.2017	21.06.2017	22.06.2017		
11	27.06.2017	28.06.2017	29.06.2017		V7E
12	04.07.2017	05.07.2017	06.07.2017		
13	11.07.2017	12.07.2017	13.07.2017		
14	18.07.2017	19.07.2017	20.07.2017		

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Example for Registration for Acceptance Test

Time Schedule for Acceptance Test

Task V4

on Tuesday & Wednesday

16.05. & 17.05.2017

Please write done your group number in a time slot of your choice.

Room is 12-211

Time slot	**Tuesday** Group No	**Wednesday** Group No
14:00 to 14:30		
14:35 to 15:05		
15:10 to 15:40		
15:45 to 16:15		
16:20 to 16:50		
16:55 to 17:25		

Grouping

- Separately for each lab
- Microelectronic Lab: grouping just done (3 students)
- Embedded Processor Lab: grouping will be done now
- Three students per group (ONE group with 4 students)
- List for grouping is distributed in this meeting; Take care of
  - Check correctness of email address
  - VHDL knowledge
  - Knowledge of Architecture of Digital Systems I (ADS I)

Access to Computers & Software

- **Tasks V1 to V3:** will be announced later

- **Room 12-274 (tasks V4-V8; task V6_E, V7_E)**

  8-11 terminals with access to server

  Opening hours: Monday to Friday from 8:00 to 18:00

  Available Server: **etana**

  Account-Names: mep_groupno e.g. mep_01

  Password: **To Be Announced**

  Required tools are installed on server etana

  Required files will be available in the account

- **Own Windows PC (tasks V4-V8) also possible**

  ModelSim and Xilinx ISE required

  Not possible for tasks V1-V3 (Mikroelektronik-Vertiefer)

  Not possible for task V6_E, V7_E (Embedded Processor Lab)

MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

Contacts EPL

Consulting on Wednesday afternoon !

Uwe Wasenmüller: wasenmueller @ eit.uni-kl.de; room 12/213
→ Organization; tasks V4 to V8; examinations

Matthias Jung: jungma @ eit.uni-kl.de; room 12/228
→ examinations V6_E, V7_E

Hans Peter Goldhammer: goldhammer @ eit.uni-kl.de; room 12/272
→ tasks V4 & V5

Eder Zulian: zulian @ eit.uni-kl.de; room 12/251
→ tasks V4, V5, V6_E & V7_E

Lab Website

- Grouping will be published on website next week
- Check website frequently

MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

Grouping: 3 students per group

- One grouping sheet for MEL – 3 students
- One grouping sheet for EPL
  - 6 groups with 3 students
  - 1 group with 4 students

- Fill out
  - Knowledge (VHDL & Architecture of digital systems)
  - Intended Degree (if not just done)
  - Students forming a group choose **same group no**

- **Check carefully your information**
  - Name
  - Email address
  - Targeted degree
  - Matrikelnumber will be inquired at first examination