Structure of sources for DLX labs

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In the following chapters the structure of the VHDL source files for DLX is shortly explained.

1. Pipeline of the DLX

This part of DLX is used in all tasks. The VHDL source files are located in /DLX/src.

- dlx_pipe_if.vhd -- Instruction Fetch Stage
- dlx_pipe_id.vhd -- Instruction Decode Stage; must be completed in task 4; must be enhanced in task 8
- dlx_pipe_ex.vhd -- Execution Stage; must be enhanced in task 8
- dlx_pipe_mem.vhd -- Memory Stage
- dlx_pipe_ctrl.vhd -- Controller of the pipeline; must be enhanced in task 5
- regfile_sim.vhd -- Simulation model of DLX registers
- dlx_pipeline.vhd – TOP Level Entity: instantiation of the previous mentioned modules

The mentioned VHDL files require the use of the following packages, which are located in /DLX/src

- dlx_global.vhd -- global constants and types; e.g. subtype opcode with 6 bit or dlx_word_s with 32 bit
- dlx_opcode_package.vhd -- Definition of OP codes and ALU function codes
- dlx_debug.vhd -- implementation of a disassemble procedure (procedure debug_disassemble); very helpful for debugging

2. Test bench for task 4 and task 5

Test bench is given by VHDL source file dlx_testbench.vhd located in /DLX/src. Test bench instantiates module dlx_pipeline. Clock signal and reset signal are properly generated. Test bench emulates the memory including the loading of the machine code. Take care, that the appropriate machine code from the directory /DLX/asm is chosen – sieb_noforw.out in task 4 and sieb_forw.out in task 5. Test bench automatically stops if the signal halt is set to '1'. This signal must be set to '1'in the ID-stage (see task 4), if a trap operation is processed. Trap command is the last machine code word in the given test programs. The test bench does **not** check the validness of the results.

3. DLX CPU

DLX CPU is **only used in task 6 to task 8**. DLX CPU consists of the module DLX_pipeline and the following VHDL source files, located in /DLX/src.

- dlx_icache.vhd -- Instruction Cache Logic
- dlx_dcache.vhd -- Data Cache Logic
- dlx_memctrl.vhd – Memory Controller
- cache_memory_sim.vhd -- Simulation model of cache memory
- dlx_cache_support.vhd – package: functions for labs with cache
- dlx_cpu.vhd – TOP Level of CPU: instantiation of previous mentioned modules and module dlx_pipeline

4. Test bench for task 6 to task 8

Test bench is given by VHDL source file dlx_cache_testbench.vhd located in /DLX/src. This test bench instantiates the module dlx_cpu. Clock signal and reset signal are properly generated. Test bench emulates the main memory including the loading of the machine code. Take care, that the appropriate machine code from the directory /DLX/asm is chosen. Test bench automatically stops if the signal halt is set to '1'. The test bench does **not** check the validness of the results.

5. Synthesis

Some tasks require performing synthesis. For these tasks all files *_sim.vhd must be replaced by the corresponding *_syn.vhd files. Furthermore the package support_pk.vhd and the file generic_dual_port_dist_ram.vhd must be used.