Towards High-Performance Reconfigurable Computing: Current challenges of a Rapid and High-Level Design Flow

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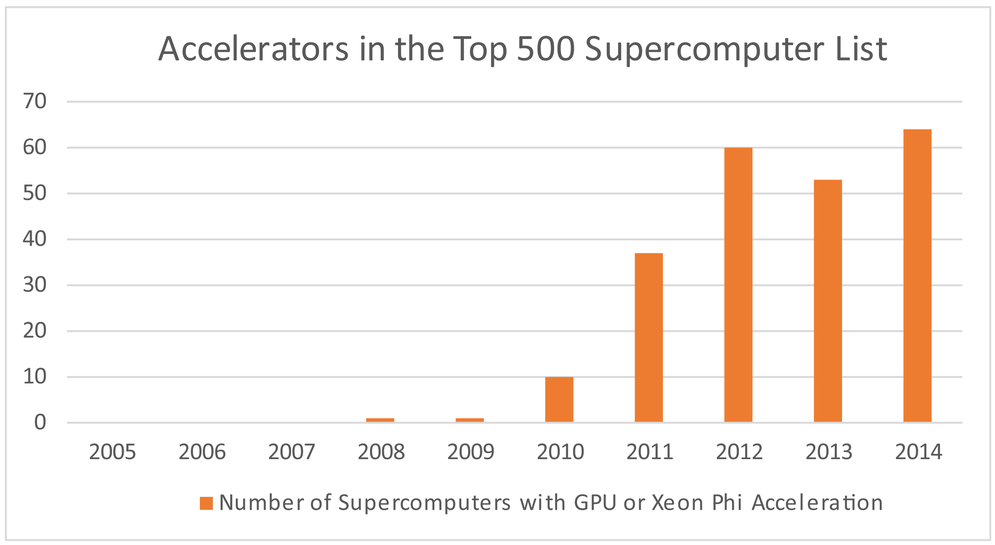
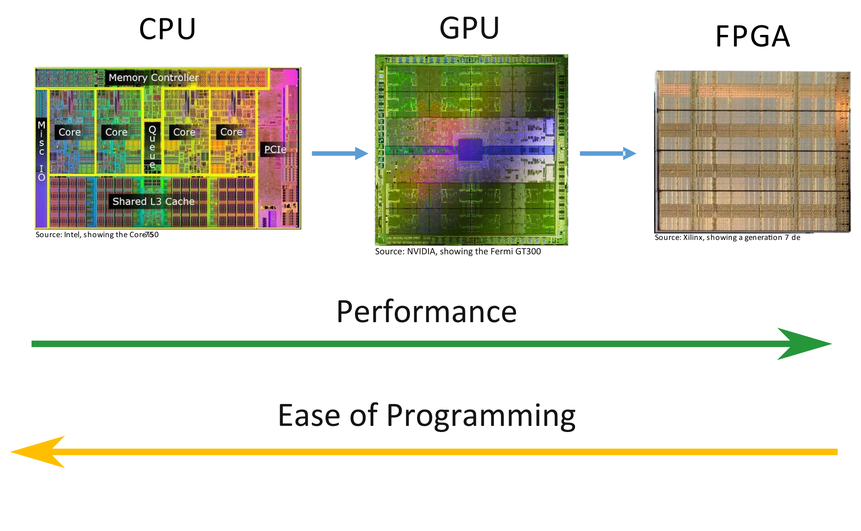
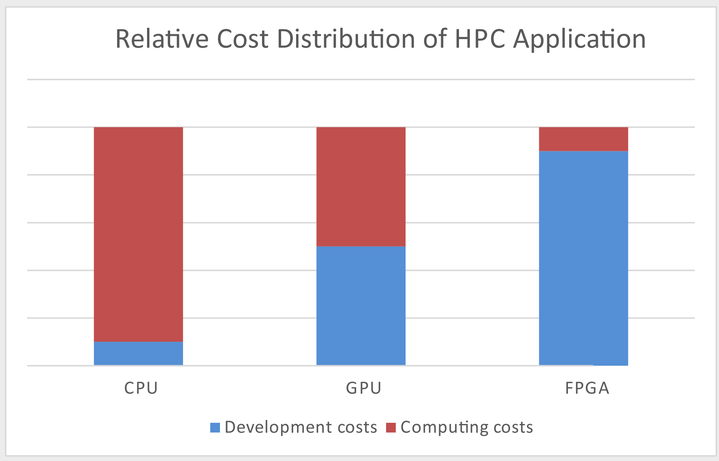
A Heterogeneous HPC World!



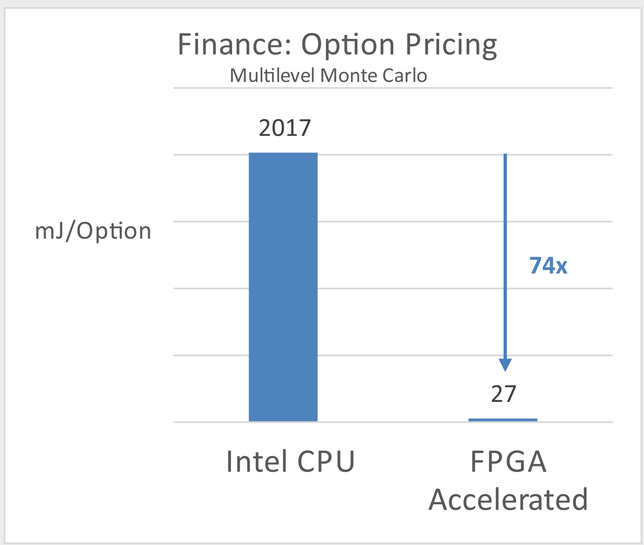


Drivers of HPC Applications

Most basically the goal in HPC is to solve complex computing problems as cheap as possible in a specific timeframe. Getting to the solution involves two major steps: programming the computing system and running the computing system. Several years ago the sweet spot for HPC computing was on one complete end of this spectrum and dominated by programmability of the architecture. Today the sweet spot has moved to more energy efficient implementation styles somewhere between CPUs and GPUs. The next established technologies beyond GPUs are FPGAs.



Huge Potential of FPGAs



CPU: Intel i5, FPGA: Xilinx Zynq 7020, European Barrier Options in the Heston model

We need Rapid Implementation Techniques for FPGAs

Education

- Code is describing **blocks in space** rather than instructions in time
- Most Algorithms taught today are a good fit to the von Neumann Architecture
- ASIC design has fundamental different goals, but often teached in instead.

Tools for Integration

- We need **abstract access** to **memory** and other computing **nodes** as todays OS provide.
- We need ready to use generators for High-Speed interfaces.
- Currently all of our developers need to be low level interface experts to debug their designs.

HLS Libraries

- We need a way to a way to design **libraries across CPU/FPGA boundaries**. As tightly coupled code is often needed.
- We need high-performance Libraries for common used design patterns.
- Currently we are reinventing the wheel a lot.

Rapid & High-Level Design Flow

CPU/FPGA Hybrid

Ubuntu Linaro

High-Level Synthesis

ABSTRACT
The HPC world is getting more and more heterogeneous. While architectures like GPUs are used for several years by now, FPGAs are not entering the HPC market so easily. Why is this the case? While it has been shown countless times that FPGA are significantly better for many applications, they are perceived to be much harder to utilize, due to high development costs. We believe that this is not inherent to FPGAs in general, but rather founded in today's established FPGA design methodologies that originally came from ASIC design. In this work we will analyze the key drivers of the HPC landscape and identify current challenges to use FPGAs for HPC. They are education, tools for system integration and missing libraries.

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