

Virtual Platforms for Fast Memory Subsystem Exploration

Using gem5 and TLM2.0

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ABSTRACT

TLM2.0 based virtual platforms are well suited for fast simulation and exploration on system level. However, for the exploration of memory subsystems, cycle accurate (CA) core models are needed, which slow down the simulation tremendously. In this paper we propose a method to playback previously recorded memory traces from the gem5 simulator in a TLM2.0 based virtual platform, to preserve simulation speed, while keeping accuracy at the same level as with cycle accurate models.

KEYWORDS: Virtual Platform, TLM2, gem5, Memory

1 Introduction

TLM2.0 based virtual platforms allow us to estimate and optimise the performance and power for different applications quickly. However, for ARM cores there is a lack of free available models. The *FastModels*, distributed by ARM Ltd. are based on *just-in-time-compilation* of the code and they use the TLM blocking coding style. Thus they do not reflect a realistic timing behaviour and can only be used for software development. Cycle accurate simulations can be done with the commercial available ARM models from Carbon Design Systems together with their SoC Designer. However, they are shipped as binary libraries with limited flexibility. Therefore, we are using the only mature cycle accurate open source system simulator *gem5* [BBB⁺11]. It is capable to simulate various ARM cores and can be adapted to our needs for the memory controller design space exploration (see Figure 1).

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2 gem5

gem5 is the result of the incorporation of the memory system simulator *GEMS* [MSB⁺05] into the former full system simulator *m5* [BDH⁺06]. gem5 is an event based simulator, programmed in the language C++. As depicted in Figure 1, gem5 has the ability to mount communication monitors between different components. These communication monitors record memory access traces and store them in compressed binary files using Google’s protocol buffer [Goo13]. A tracefile consist of packets with information about time, command and address, shown in Listing 1.

```
message Packet {  
  required uint64 tick = 1;  
  required uint32 cmd = 2;  
  required uint64 addr = 3;  
  required uint32 size = 4;  
  optional uint32 flags = 5;  
  optional uint64 id = 6;  
}
```

Listing 1: Protobuf definition

3 TLM2.0 based Virtual Platform

To use this trace files in a TLM2.0 based virtual platform, we developed a trace player based on the approximately timed coding style. This trace player is interoperable and can be used in any TLM2.0 based virtual platform.

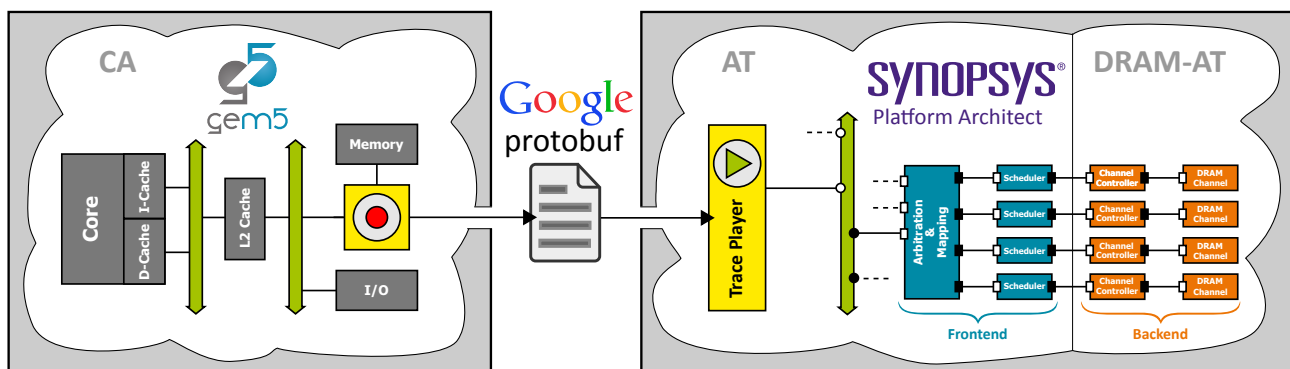


Figure 1: A Typical Setup for Trace-Based Virtual Platforms

Figure 1 shows an example for such a platform created with Synopsys Platform Architect. This platform, presented in [JWWC13] and [JWB⁺13] is used for the design space exploration of the 3D-DRAM memory controller frontend. The backend part of the controller was already investigated in [WLBW12, WLBW13].

4 Conclusion

Based on our practical experiments, the proposed approach is more than 150x faster than near cycle-accurate simulations and only ten times slower than real-time. For instance a trace with the length of 4 seconds can be simulated in 40 seconds. Using this method we are able to perform a large number of simulations with different parameter values in a very fast way.

References

- [BBB⁺11] Nathan Binkert, Bradford Beckmann, Gabriel Black, Steven K. Reinhardt, Ali Saidi, Arkaprava Basu, Joel Hestness, Derek R. Hower, Tushar Krishna, Somayeh Sardashti, Rathijit Sen, Korey Sewell, Muhammad Shoaib, Nilay Vaish, Mark D. Hill, and David A. Wood. The gem5 simulator. *SIGARCH Comput. Archit. News*, 39(2):1–7, August 2011.
- [BDH⁺06] Nathan L. Binkert, Ronald G. Dreslinski, Lisa R. Hsu, Kevin T. Lim, Ali G. Saidi, and Steven K. Reinhardt. The m5 simulator: Modeling networked systems. *IEEE Micro*, 26:52–60, 2006.
- [Goo13] Inc. Google. Protocol Buffers - Google’s Data Interchange Format. <https://code.google.com/p/protobuf/>, May 2013.
- [JWB⁺13] Matthias Jung, Christian Weis, Patrick Bertram, Gunnar Braun, and Norbert Wehn. Power Modelling of 3D-Stacked Memories with TLM2.0 Based Virtual Platforms. In *Proceedings of Synopsys Usergroup Conference, SNUG ’13*. Synopsys, 2013.
- [JWWC13] Matthias Jung, Christian Weis, Norbert Wehn, and Karthik Chandrasekar. TLM Modelling of 3d Stacked Wide I/O DRAM Subsystems: A Virtual Platform for Memory Controller Design Space Exploration. In *Proceedings of the 2013 Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools, RAPIDO ’13*, pages 5:1–5:6, New York, NY, USA, 2013. ACM.
- [MSB⁺05] Milo M. K. Martin, Daniel J. Sorin, Bradford M. Beckmann, Michael R. Marty, Min Xu, Alaa R. Alameldeen, Kevin E. Moore, Mark D. Hill, and David A. Wood. Multifacet’s general execution-driven multiprocessor simulator (gems) toolset. *SIGARCH Comput. Archit. News*, 33(4):92–99, November 2005.
- [WLBW12] C. Weis, I. Loi, L. Benini, and N. Wehn. An energy efficient dram subsystem for 3d integrated socs. In *Design, Automation Test in Europe Conference Exhibition (DATE), 2012*, pages 1138–1141, 2012.
- [WLBW13] C. Weis, I. Loi, L. Benini, and N. Wehn. Exploration and Optimization of 3-D Integrated DRAM Subsystems. *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, 32(4):597–610, 2013.